IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 13782US03)

In the Application of:

Uri Elzur, et al.

Serial No. 10/652,267

Filed: August 29, 2003

For: SYSTEM AND METHOD FOR TCP OFFLOAD

Examiner: Avellino, Joseph E.

Group Art Unit: 2143

Confirmation No. 1986

REPLY BRIEF

MS: APPEAL BRIEF-PATENTS
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 CFR 41.41, the Appellant submits this Reply Brief in response to the Examiner's Answer mailed on July 3, 2006. Claims 1-33 are pending in the present Application. The Appellant has responded to the Examiner in the Examiner's Answer, as found in the following Argument section.

As may be verified in his final Office Action (page 2), dated October 7, 2005 ("Final Office Action"), the Examiner had previously rejected claims 1-5 and 7-33 under 35 U.S.C. § 102(e) as being anticipated by Boucher, et al., U.S. Patent No.

6,757,746 ("Boucher"). In his Final Office Action (page 4), the Examiner also rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Boucher. To aid the Board in identifying corresponding arguments, the Appellant has used the same headings in the Argument section of this Reply Brief as the headings found in the Appellant's corresponding Brief on Appeal. The Brief on Appeal has a date of deposit of May 15, 2006.

STATUS OF THE CLAIMS

Claims 1-33 were finally rejected. Pending claims 1-33 are the subject of this appeal.

ARGUMENT

I-A. Boucher Does Not Teach or Suggest "Processing Occurring Without Reassembly"

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellants' Brief on Appeal, the Examiner states the following on pages 7-8 of the Examiner's Answer:

> The Examiner has clearly shown that the [Applicant's] specification teaches (page 11, ¶39) that **reassembly is dealing with reassembling TCP/IP packets which were fragmented**...Reassembling data, as limited by the specification, deals **only with reassembling fragmented packets** (see cited portions of the specification above). (Emphasis added)

The Appellant disagrees. The Examiner is apparently asserting that the Applicant uses the term "reassembly" only for fragmented data packets. The Examiner obviously infers that since Boucher teaches reassembly of non-fragmented data and since the Applicant allegedly discloses reassembly of only fragmented data, then Boucher does in fact teach "processing occurring without reassembly." The Applicant disagrees with this argument and submits that the Examiner's reasoning is erroneous.

More specifically, the relevant portion of the Appellant's specification cited by the Examiner (page 11, ¶39) states the following:

> Additionally, a NIC in accordance with an embodiment of the invention *will not comprise a dedicated memory which is to be*

> *utilized for reordering or reassembling out-of-sequence TCP packets or IP fragments*. Furthermore, in accordance with an embodiment of the invention, the NIC will not include a large TOE dedicated memory that is utilized for packet retransmission and/or packet reassembly. Accordingly, no packet reassembly and/or packet retransmission buffering need be done by a TCP enabled Ethernet controller (TEEC). (Emphasis added)

The Appellant points out that no where in the above citation of ¶39 of the Appellant's specification is it stated that reassembling "deals only with reassembling fragmented packets," as argued by the Examiner. The Examiner is referred to the first sentence of the above citation of ¶39 of the Appellant's specification, clearly showing that "reassembly" may apply to IP fragments or TCP packets, for example. In other words, **"reassembly" does not necessarily apply to only fragmented data**, as argued by the Examiner. Therefore, the Appellant submits that the term "reassembly" in Appellant's claim 1 applies to **both** fragmented as well as non-fragmented data.

In response to Appellants' Brief on Appeal, the Examiner further states the following on page 8 of the Examiner's Answer:

> Appellant should be aware that ***"assembling" data and "reassembling" data is not the same***...The packets are "assembled" in the NIC card of Boucher by clocking in specific bits of data in order to correctly route/forward the packet (See Boucher '173, col. 27, lines 12-15, the register is a "shift register 2217" wherein data is loaded serially a single byte at a time and is unloaded in parallel). This is what Appellant is attempting to equate to the claimed "processing without reassembly". (Emphasis added)

The Examiner has acknowledged that **packets are assembled** in the ASIC 400 of Boucher. However, Boucher '173 states that "data shifted into register 2217 (which is within ASIC 400) is examined at the register outputs by protocol analyzer 2203 (which is also within the ASIC 400) which verifies checksums, and generates "status" information 2223." *See* Boucher '173, column 27, lines 32-35. In this regard, the protocol analyzer 2203 of Boucher '173 performs functionalities, such as checksum verification, which is indicative that the ASIC 400 reassembles fragmented packets, contrary to the Examiner's assertions. Boucher, therefore, discloses reassembling of fragmented packets. In this regard, Boucher does not disclose "processing occurring without reassembly," as claimed by the Appellant in claim 1.

In addition, the Appellant disagrees with the Examiner's assertion that "assembling" data and "reassembling" data is not the same, in light of the Boucher reference. The Appellant submits that "assembly" and "reassembly" of data are indeed the same, in light of the Boucher reference. For example, the data assembly register 2202 of Boucher is *located within the* ***receive*** *sequencer* 2105. Obviously, the receive sequencer 2105 receives network data communicated to the ASIC 400. In other words, network data communicated to the receive sequencer 2105 has originated somewhere else and has been fragmented somewhere else (at the transmit site for example) prior to being received by the ASIC 400. Therefore, **"assembling" received data within the**

receive sequencer 2105 is the same as "reassembling" the received data, as the received data is obviously fragmented network data that is being assembled back (or reassembled) by the ASIC 400 of Boucher. In this regard, the ASIC 400 of Boucher discloses processing of data which occurs with assembly (which for received network data is the same is "reassembly"). Boucher, therefore, does not disclose or suggest "processing occurring without reassembly," as claimed by the Appellant in claim 1.

The Appellant respectfully submits that claims 1, 16, and 25 are allowable.

I-B. Boucher Does Not Teach Or Suggest "A TEEC Including At Least One Internal Elastic Buffer, Wherein The TEEC Processes An Incoming TCP Packet Once And Temporarily Buffers At Least A Portion Of Said Incoming TCP Packet In Said Internal Elastic Buffer"

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellants' Brief on Appeal, the Examiner states the following on page 8 of the Examiner's Answer:

> Appellant has not sufficiently defined what is meant by an "elastic buffer". The Examiner equates the claimed "elastic buffer" to the data synchronization buffer 2200 on the ASIC chip as found in Boucher '173 (Figure 21 shows the ASIC 400 encompasses the receiving sequencer 2105; as shown in Figure 22, the data sync buffer 220 is clearly within the receiving sequencer 2105 and is therefore on the ASIC 400).

The Appellant disagrees and continues to maintain that the term "elastic buffer" and its functionality are sufficiently well defined in light of the specification and the claims.

Assuming for the sake of argument that the data synchronization buffer 2200 is an elastic buffer, which the Applicant submits it is not, Boucher still *does not disclose or suggest that the ASIC 400 processes an incoming buffer and then buffers at least a portion of the TCP packet in the elastic buffer*, as recited, for example, in claim 1 of the present application. Boucher simply does not disclose or suggest any packet processing prior to the data being buffered in the synchronization buffer 2200.

The Appellant respectfully submits that claims 1, 16, and 25 are allowable.

I-C. Rejection of Claim 2 under 35 U.S.C. § 102(e)

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

In response to Appellants' Brief on Appeal, the Examiner states the following on page 9 of the Examiner's Answer:

> [T]he data sync buffer stores packets as they are being received. Any packet received is transmitted to the host memory to be reassembled, and therefore can be construed as the transmit internal elastic buffer as well. Therefore the data sync register can be both the receiving and transmitting internal elastic buffer.

The Applicant disagrees with this argument at least for the reasons stated in the Brief on Appeal. The Applicant is puzzled as to how a data synchronization buffer (2200), which is located within the Receive Sequencer (2105) of ASIC 400 and which only processes received data, may be used as a transmit elastic buffer for transmit data. The Applicant submits that this is not possible. For example, the Examiner is urged to reference Figure 21 of Boucher, where Boucher has clearly separated processing of received data only by the receive sequencer 2105, and processing of outgoing, or transmit data, by the transmit sequencer 2104. If the above argument by the Examiner were true, then there would be no need for the transmit sequencer 2104. Clearly, this is not the case and, therefore, the Examiner's argument is erroneous.

The Appellant respectfully submits that claim 2 is allowable.

I-D. Rejection of Claims 3 and 4 under 35 U.S.C. § 102(e)

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that claims 3 and 4 are allowable.

I-E. Rejection of Claim 5 under 35 U.S.C. § 102(e)

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section and he continues to rely on Figure 2 of Boucher. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

It is unclear why the Examiner is referring to Figure 2 of Boucher since this figure does not disclose that the NIC places at least a portion of incoming TCP data into a portion of the host memory. Figure 2 of Boucher discloses transferring a portion of *already processed* multi-packet session layer message 200 to the host, and does not disclose transferring of incoming TCP data, as claimed by the Appellant.

The Appellant respectfully submits that claim 5 is allowable.

I-F. Rejection of Claim 7 under 35 U.S.C. § 102(e)

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal as well as the arguments in Section I-E above.

The Appellant respectfully submits that claim 7 is allowable.

I-G. Rejection of Claim 8 under 35 U.S.C. § 102(e)

In response to Appellant's Brief on Appeal, the Examiner continues to maintain that "the NIC card (200) does not require dedicated memory to conduct such reordering" and "data is automatically DMA'd over to the host memory."

The Appellant disagrees. The Examiner is referred to Figure 21 of Boucher '173 and the fact that the ASIC 400, which the Examiner equates to the TEEC, is utilizing the DRAM 460 (which is within the NIC 200) for processing, and not the host memory. The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that claim 8 is allowable.

I-H. Rejection of Claims 10-13 under 35 U.S.C. § 102(e)

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that claims 10-13 are allowable.

I-I. Rejection of Claim 14 under 35 U.S.C. § 102(e)

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that claim 14 is allowable.

II. Inherency

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section. The Examiner continues to rely on Figure 2 of Boucher and has not addressed the Appellant's argument made in the Brief on Appeal. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that claim 9 is allowable.

III. Boucher Does Not Render Claim 6 Unpatentable

In response to Appellant's Brief on Appeal, the Examiner has not stated any new arguments as it relates to this section. Therefore, the Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

The Appellant respectfully submits that claim 6 is allowable.

CONCLUSION

The Appellant submits that the pending claims are allowable in all respects. Reversal of the Examiner's rejections for all the pending claims and issuance of a patent on the Application are therefore requested from the Board.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Date: 25-AUG-2006 By: _____

Ognyan Beremski, Reg. No. 51,458
Attorney for Appellant

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8000
Facsimile: (312) 775 – 8100